₹ 200 ISSN - 2249-555X
Volume : 1 Issue : 9 June 2012

Indian Journal Of Applied Research

Journal for All Subjects

www.ijar.in

Listed in International ISSN Directory, Paris.

ISSN - 2249-555X

Indian Journal of Applied Research

Journal for All Subjects

Advertisement Details

Position	B/W (Single Color)	Fore Color
Full Inside Cover	₹ 6000	₹ 12500
Full Page (Inside)	₹ 5000	-

Subscription Details

Period	Rate	Discount	Amount Payable
One Year (12 Issues)	₹ 2400	Nil	₹ 2400
Two Year (24 issues)	₹ 4800	₹ 200	₹ 4600
Three Year (36 issues)	₹ 7200	₹ 300	₹ 6900
Five Year (60 issues)	₹ 12000	₹ 600	₹ 11400

You can download the Advertisement / Subscription Form from website www.ijar.in. You will require to print the form. Please fill the form completely and send it to the **Editor, INDIAN JOURNAL OF APPLIED RESEARCH** along with the payment in the form of Demand Draft/Cheque at Par drawn in favour of **INDIAN JOURNAL OF APPLIED RESEARCH** payable at Ahmedabad.

1. Thoughts, language vision and example in published research paper are entirely of author of research paper. It is not necessary that both editor and editorial board are satisfied by the research paper. The responsibility of the matter of research paper/article is entirely of author.
2. Editing of the Indian Journal of Applied Research is processed without any remittance. The selection and publication is done after recommendations of atleast two subject expert referees.
3. In any condition if any National/International University denies accepting the research paper published in IJAR, then it is not the responsibility of Editor, Publisher and Management.
4. Only the first author is entitle to receive the copies of all co-authors
5. Before re-use of published research paper in any manner, it is compulsory to take written permission from the Editor-IJAR, unless it will be assumed as disobedience of copyright rules.
5. All the legal undertaking related to Indian Journal of Applied Research is subject to Ahmedabad Jurisdiction.
7. The research journal will be send by normal post. If the journal is not received by the author of research papers then it will not be the responsibility of the Editor and publisher. The amount for registered post should be borne by author of the research paper in case of second copy of the journal.

Editor,
Indian Journal Of Applied Research
8-A, Banans, Opp. SLU Girls College, New Congres Bhavan, Paldi,
Ahmedabad-380006, Gujarat, INDIA
Contact.: +91-9824097643 E-mail : editor@ijar.in

INDEX

Volume : 1 | Issue : 9 | June 2012 ISSN - 2249-555X

Research Paper Engineering

Hardware modeling Simulation with COSSAP

* Krunali Amrutlal Ratanpara ** Devendra Soni
*** Shrenik Rajesh Golwelkar

*,**,*** Assistant Professor, Amc Engineering College, Bangalore

ABSTRACT

The paper describes the integration of an experimental test system for digital signal processing hard-ware into a data ow driven system simulation environment. The integration enables running simulations with actual hardware components \in the loop" (hardware modeling). The implications of data own driven simulations to hardware modeling are discussed as compared to hardware modeling in conjunction with event driven simulation. The experimental setup is described and results for the achieved simulation speedup are given.

INTRODUCTION

The integration of telecommunication systems on silicon is currently facing major challenges due to the fast progress in technology. Today, managing design complexity has be-come the limiting factor rather than circuit technology. Thus ad-vanced design methodologies have become a pre-requisite to be capable of designing VLSI systems which make ancient use of the technological opportunities. As one consequence, the development of heterogeneous simulation environments (e.g. mixed mode simulation) has recently attracted increased attention [1] [4].

As a facet of heterogeneous simulations we discuss in this pa-per simulations which employ actual hardware components. In the sequel the resulting simulation is called hardware in the loop simulation and the modeling technique hardware modeling. Hardware modeling was introduced by Widdoes in 1984 [6].

Experiments have proven that data flow simulation provides speedups in excess of one order of magnitude as compared to event driven simulation which is predominantly used on lower levels of abstraction [1,5].

There are several advantages resulting from the use of digital signal processing hardware whose input is comput-ed by a simulation program running on a workstation and whose out-put is read in by the same program:

Authenticity:
The piece of hardware is the same as in the target system this guarantees perfect authenticity of the simulation results as far as the included piece of hardware is concerned.

Modeling:
In case hardware components are purchased from external suppliers, system development is possible even with the ba-sic black-box knowledge about these components since this information is sauciest for hardware modeling.

Well Defined Verification Environment:
Hardware components can be varied against the specification in a well defined environment. The data fed to the hardware board can either be straightforward for debugging purposes or very complex resulting from comprehensive system model implemented in the simulation system.

HARDWARE MODELING AND DATA FLOW SIMULATION

We will briefly introduce the concept of a signal in a data flow driven simulation in this section to prepare the ground for a clear discussion of advantages and limitations of hardware modeling in the context of a data flow driven simulation.

Signal Paradigms
Hardware modeling requires the generation of all physical signals that are required to run the hardware control-led by the simulation. A signal paradigm defines. The relation of the value of a signal to the on going (virtual) simulation time At which time a simulation model is fired to compute new values of its output signals (module scheduling).

Different signal paradigms reject different levels of abstraction of a physical signal which exhibit a value at every point of time and are thus not generally representable in a digital computer.

Table 1. Signal Paradigms

Signal paradigm	Signal/time relation	Scheduling scheme	Used in
Event driven	Value & time of change	Chang of an input signal	VHDL etc
Data ow driven	Only sequence of value	All necessary input samples value	COSSAP etc.

Event driven simulations are based on the idea that a signal can be described by a sequence of events which describe a signal change. The fired model then computes the new val-ues of its output signals. The associated events are inserted into an event table which is managed by the kernel of the simulator.

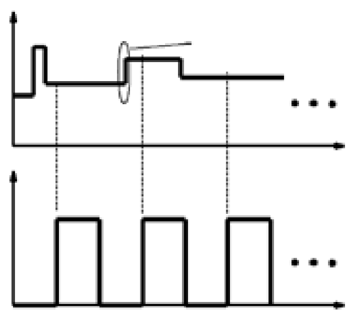

Fig. 1: Event driven signal representation

Data flow simulations, in contrast, do not keep track of the time. Signals are represented merely by sequences of values. The sequence does not even necessarily have an interpreta-tion on the time axis. The values may equally well describe for example signals in the frequency domain or asynchronous signals [13].

In contrast to event driven simulation control signals are not required to model systems in a data flow driven simulation since the sequence of values is sufficient to drive most algorithms in digital signal processing. However, whenever interfacing to real world signals is required an interpretation over time must be added to the data flow signals.

Interfacing to Physical Signals
Physical signals are obviously not directly interfaceable to a data flow signal since they continuously exhibit a value at each time instant. Consequently sampling of these signals is required to interface to the simulation.

Digital hardware usually either runs at a fixed clock rate which in turn defines at what time meaningful signal values at the ports are present or establishes explicit handshaking schemes. Such devices .As a advantage of the latter case multiple instances of the device in a simulation can be handled if the stimuli history is stored for each instance. Clearly, supporting dynamic components and multiple instances leads to very complex interfaces with high speed memory, programmable clock sources etc.

Interface Model Requirements
It is of course desirable to provide a hardware model at the system level to the design engineer which resembles the hardware in a form that allows easy integration into the system simulation setup.

A primitive model 1 in COSSAP is a model written in a programming language like C which communicates via well defined interface functions to other models. In order to be easy and convenient to use, the interface model should comprise the following functionality:

Universality:
The interface model should be parametrizable to serve arbitrary hardware hooked on the hardware interface.

Initialization:
The interface model should provide a pos-sibility to initialize the hardware and the hardware interface, since explicit signal generation for initialization in the simulation setup can be very awkward.

Signal Hiding:
The interface model should be capable of applying simple clock systems, and constant signal values to the hardware without requiring equivalent data flow signals, since these signals are often not required for the remaining simulation.

A SAMPLE SOLUTION
We developed a primitive model for the system simulator COSSAP and a proprietary hardware interface at our institute which allows us to model hardware mainly for systems and ASICs developed in our institute.

ISS Test Hardware

As was elaborated earlier the complexity of the interface hardware is determined to a large degree by the hardware which is to be included into the simulation setup. The interface complexity may range from simple programmable parallel interface to complex hardware which may be required to satisfy absolute timing requirements

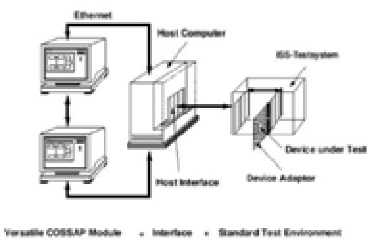

Fig. 2: ISS Test Hardware

The test hardware at our institute was developed for low cost testing of fully synchronous digital hardware. The test hardware consists of 160 programmable interface pins, a

Programmable clock generator which provides three clock signals of up to 50MHz frequency and a programmable cycle counter which allows to apply clock bursts of up to 224 cycles to the device under test

A Versatile Interface Model
A versatile COSSAP module has been developed which is configurable for any device adaptor. The module takes a data set for module configuration [16]. Hardware initialization is performed in the aforementioned manner.

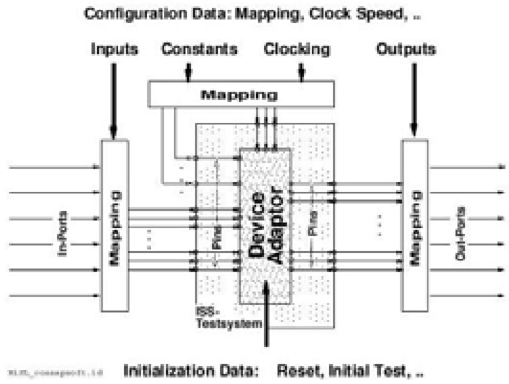

Fig. 3: Structure of the COSSAP Module

The data set which configures the model has four parts which establish input mapping, output mapping and interpretation, constant signal specification and clock specification. A mapping specification establishes a mapping between a data flow signal (of type integer) at port number N to one or more bits of the hardware interface.

Performance
In the following we discuss as an example the simulation of the experimental fully digital 100MBit/s receiver DIRECS [13], which consists of 6 ASICs. Figure 6 shows the hierarchical software model of the receiver which consists of several primitive models.

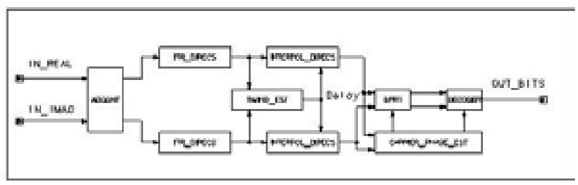

Fig. 4: Hierarchical COSSAP Model of DIRECS

It is worth mentioning here that the model in Figures 6 has different data rates at inputs and outputs since a digital receiver usually requires oversampling of the input signals.

By runtime profiling of our software, it was found that the bandwidth of the host interface limits the simulation throughput of our example. However, even in the small simulation setup described above, the interface software to our testing environment consumed only 20% of the simulation runtime which shows that optimization of this interface would not result in large speedups. After all, the verification of the receiver was made possible down to bit error rates of 10 7 due to a tenfold increase in simulation efficiency as compared to the software models of Figure 4. The resulting number of 250 million clock cycles (17 Gigabits of data) shows clearly why playing stimuli historys was not a viable solution for our application.

CONCLUSION

While hardware modeling in conjunction with event driven simulation is a commercial reality, our experimental setup shows that hardware modeling is possible in conjunction with data flow driven simulations. This is due to the fact that we deal with the sequence of meaningful values rather than timed signals. We did not support bidirectional ports. These restrictions react our application domain which is in the loop simulation of digital signal processing ASICs. An experimental hardware modeling solution for the simulation system COS-SAP was developed in conjunction with a proprietary test environment for integrated circuits and VLSI systems. This solution provides the full functionality for hardware modeling of the hardware components at high simulation speed and low cost.

REFERENCES

[1] P. Zepter and K. ten Hagen, \Using VHDL with stream driven simulators for digital signal processing applicati-ons," in EURO-VHDL'91 Proceedings, (Stockholm, Swe-den), pp. 196{203, September 8-11 1991. | | [2]\Simbus simulation backplane." Product Information, Vie-wLogic Inc., 1993. | | [3]G. Jennings, \A case against event driven simulation of digital system design," in The 24th Annual Simulation Symposium (A. H. Rutan, ed.), (Los Alamitos, California), pp. 170{176, IEEE Computer Society Press, April 1991. | | [4]L. Widdoes and W. Harding, \CAE station uses real chips to simulate VLSI-based systems," Electronic Design, vol. 32, pp. 167{76, March 1984. | | [5] [8] J. Kunkel, \COSSAP: A stream driven simulator," in | [6]IEEE International Workshop on microelectronics in | [7] Communication Switzerland, March 1991.

Sara Publishing Academy
Indian Journal Of Applied Research
Journal for All Subjects

Editor,
Indian Journal Of Applied Research
8-A, Banans, Opp. SLU Girls College,
New Congres Bhavan, Paldi, Ahmedabad-380006.
Contact.: +91-9824097643 E-mail : editor@ijar.in

Printed at Unique Offset, Novatsing Rupam Estate, Opp. Abhay Estate, Tavdipura, Shahibaug, Ahmedabad